DATA SHEET

74LVT543

3.3V Octal latched transceiver with dual enable (3-State)

Product specification
Supersedes data of 1994 May 20
IC23 Data Handbook

1998 Feb 19

Philips
Semiconductors

PHILIPS

3.3V Octal latched transceiver with dual enable (3-State)

74LVT543

FEATURES

- Combines 74LVT245 and 74LVT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64mA/–32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT543 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

FUNCTIONAL DESCRIPTION

The 74LVT543 contains two sets of eight D–type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($\overline{EAB}$) input and the A-to-B Latch Enable ($\overline{LEAB}$) input are Low the A-to-B path is transparent. A subsequent Low-to-High transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

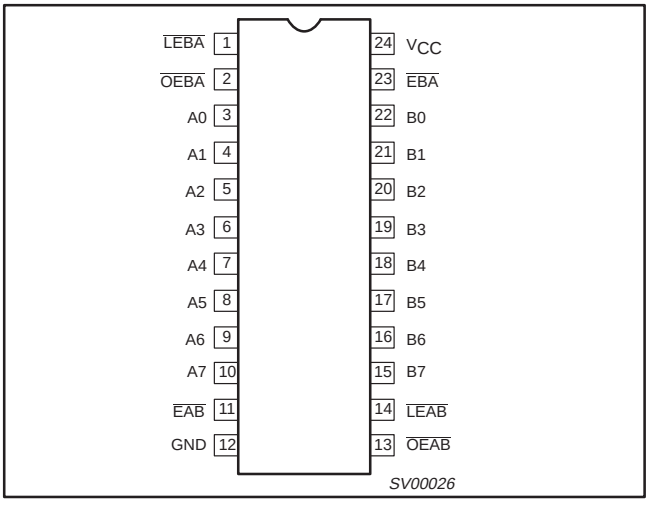
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 3.3V	2.3 3.0	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	10	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

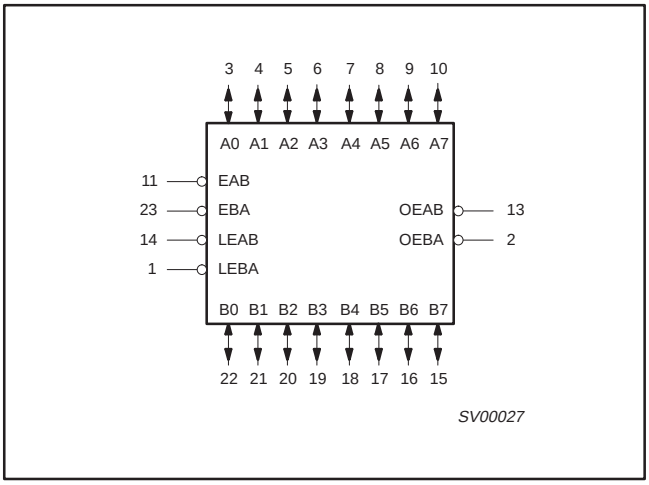
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic SOL	–40°C to +85°C	74LVT543 D	74LVT543 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT543 DB	74LVT543 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT543 PW	74LVT543PW DH	SOT355-1

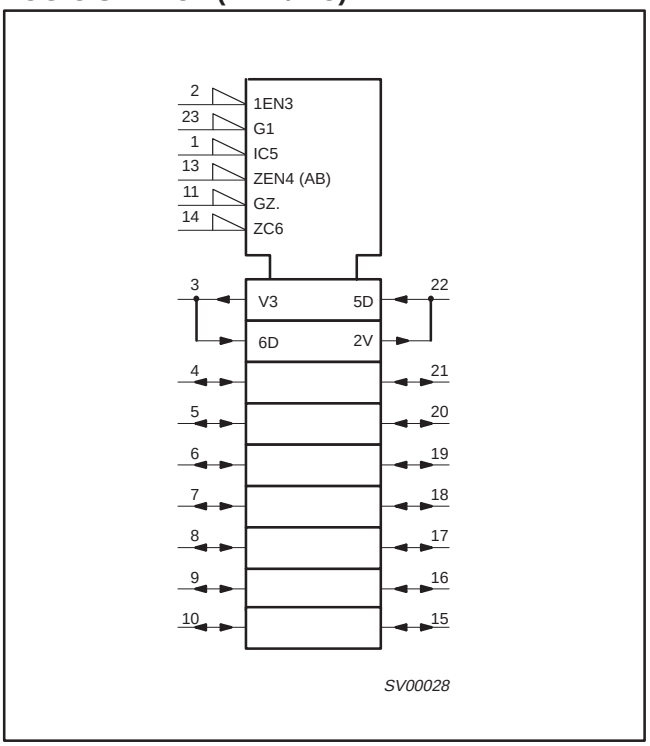
PIN CONFIGURATION



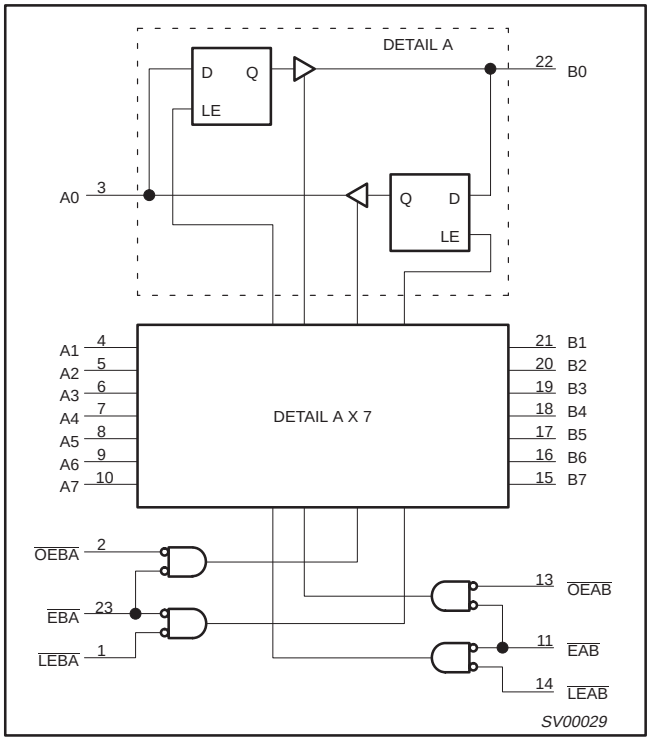
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
14, 1	$\overline{LEAB}$ / $\overline{LEBA}$	A to B / B to A Latch Enable input (active-Low)
11, 23	$\overline{EAB}$ / $\overline{EBA}$	A to B / B to A Enable input (active-Low)
13, 2	$\overline{OEAB}$ / $\overline{OEBA}$	A to B / B to A Output Enable input (active-Low)
3, 4, 5, 6, 7, 8, 9, 10	A0 – A7	Port A, 3-State outputs
22, 21, 20, 19, 18, 17, 16, 15	B0 – B7	Port B, 3-State outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	An or Bn	Bn or An	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX = AB or BA)
NC = No change
Z = High impedance or "off" state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	
		V_{CC} = 3.6V; V_I = 5.5V	I/O Data pins[4]		1	20	
		V_{CC} = 3.6V; V_I = V_{CC}			0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[6]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			15	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC} -0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
6. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	2	1.0 1.0	2.3 3.0	4.7 4.6	5.5 5.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	1 2	1.0 1.0	3.6 4.2	5.9 5.7	7.3 7.3	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	4 5	1.0 1.1	3.8 3.8	5.8 6.4	7.6 8.2	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	4 5	2.4 2.0	3.7 3.5	6.5 5.8	7.1 5.9	ns
t_{PZH} t_{PZL}	Output enable time $\overline{EBA}$ to An, $\overline{EAB}$ to Bn	4 5	1.0 1.4	4.0 4.1	6.0 6.7	7.6 8.3	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{EBA}$ to An, $\overline{EAB}$ to Bn	4 5	2.3 2.0	3.7 3.5	6.4 5.4	7.1 5.6	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

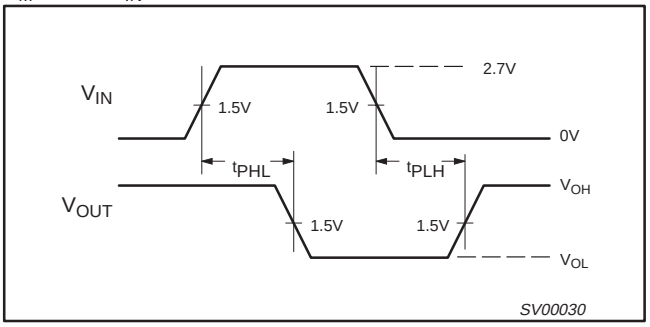
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

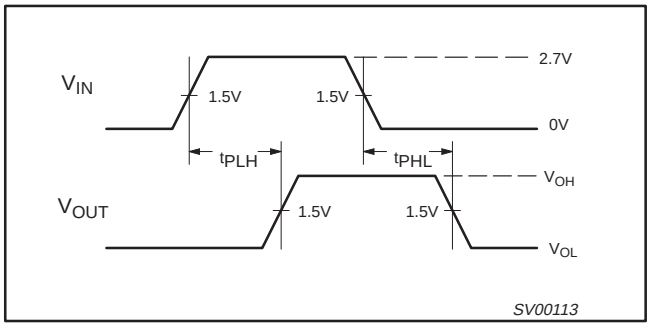
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V	
			MIN	MAX	MIN	
t_s(H) t_s(L)	Setup time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	3	0 0.8		0 1.1	ns
t_h(H) t_h(L)	Hold time An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	3	1.7 1.7		1.7 1.7	ns
t_s(H) t_s(L)	Setup time An to $\overline{EAB}$, Bn to $\overline{EBA}$	3	0 0.9		0 1.2	ns
t_h(H) t_h(L)	Hold time An to $\overline{EAB}$, Bn to $\overline{EBA}$	3	1.8 1.8		1.8 1.8	ns
t_w(L)	Latch enable pulse width, Low	3	3.3		3.3	ns

AC WAVEFORMS

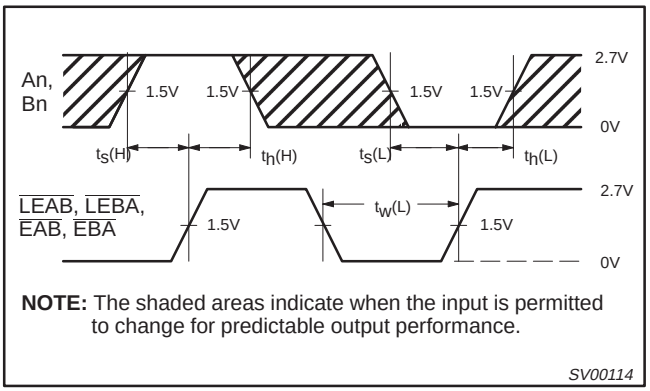
V_M = 1.5V, V_{IN} = GND to 2.7V



Waveform 1. Propagation Delay For Inverting Output

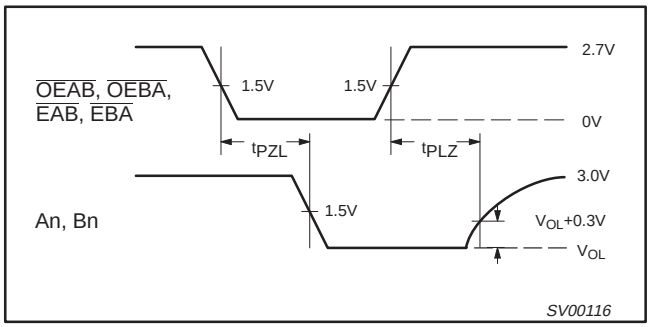


Waveform 2. Propagation Delay For Non-Inverting Output

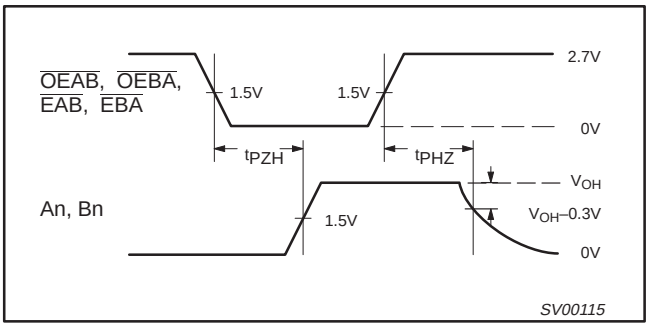


NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3. Data Setup and Hold Times And Latch Enable Pulse Width

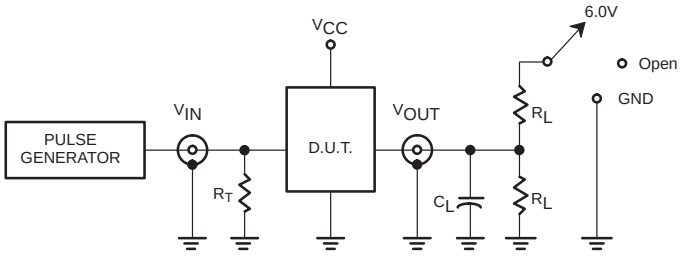


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

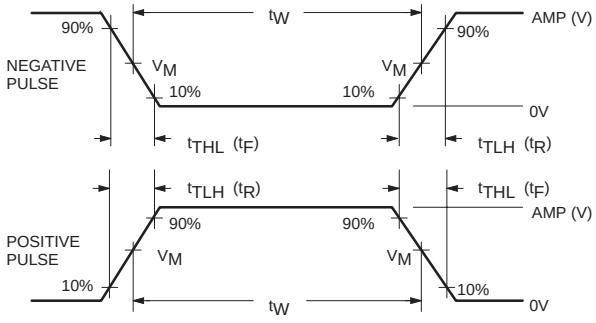


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

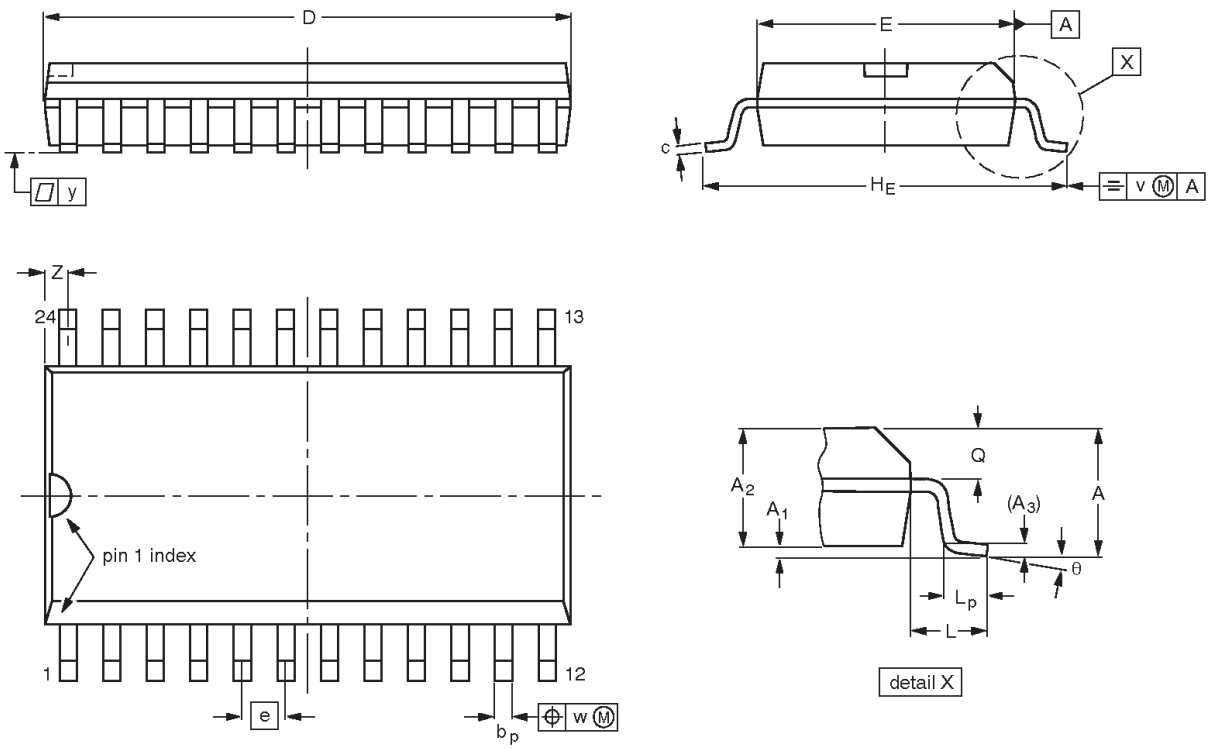
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

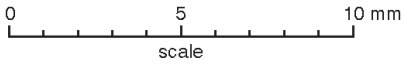
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SV00092

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

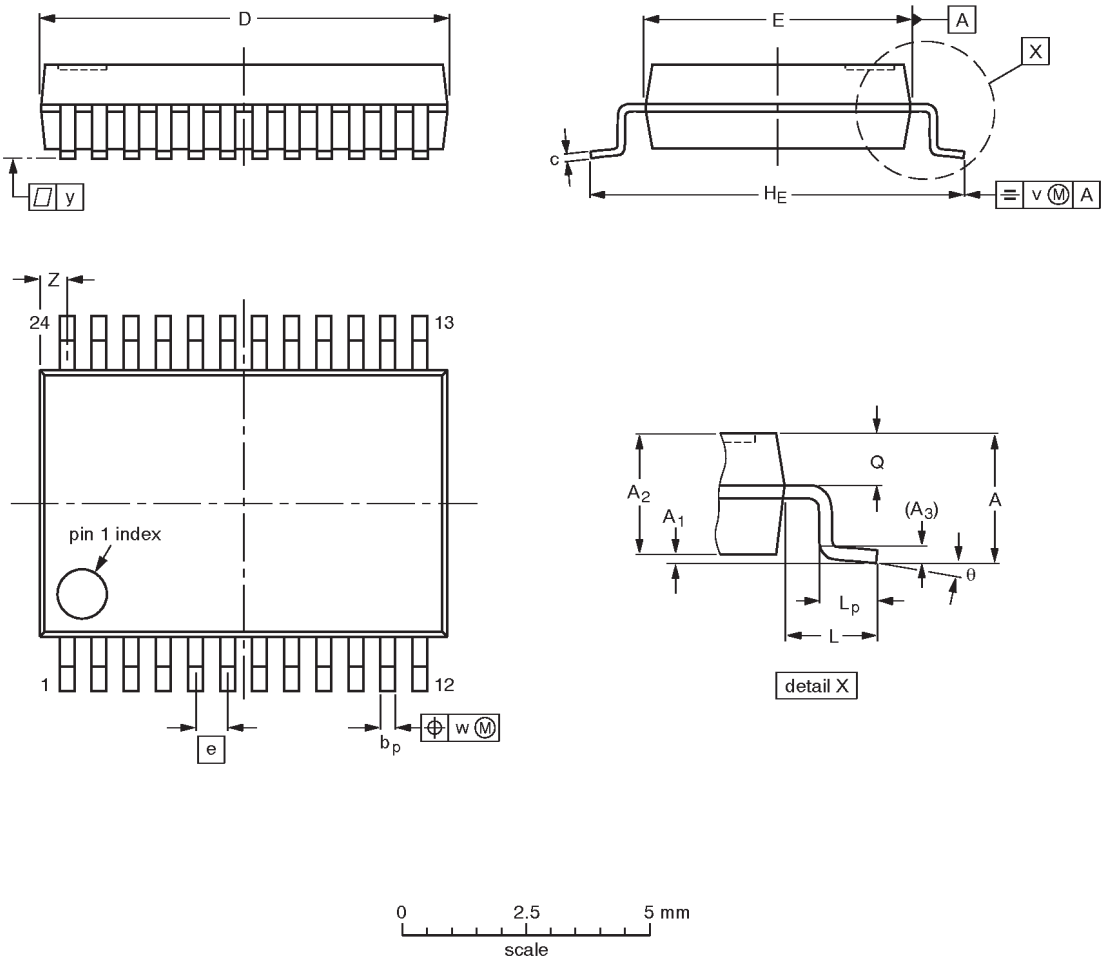
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

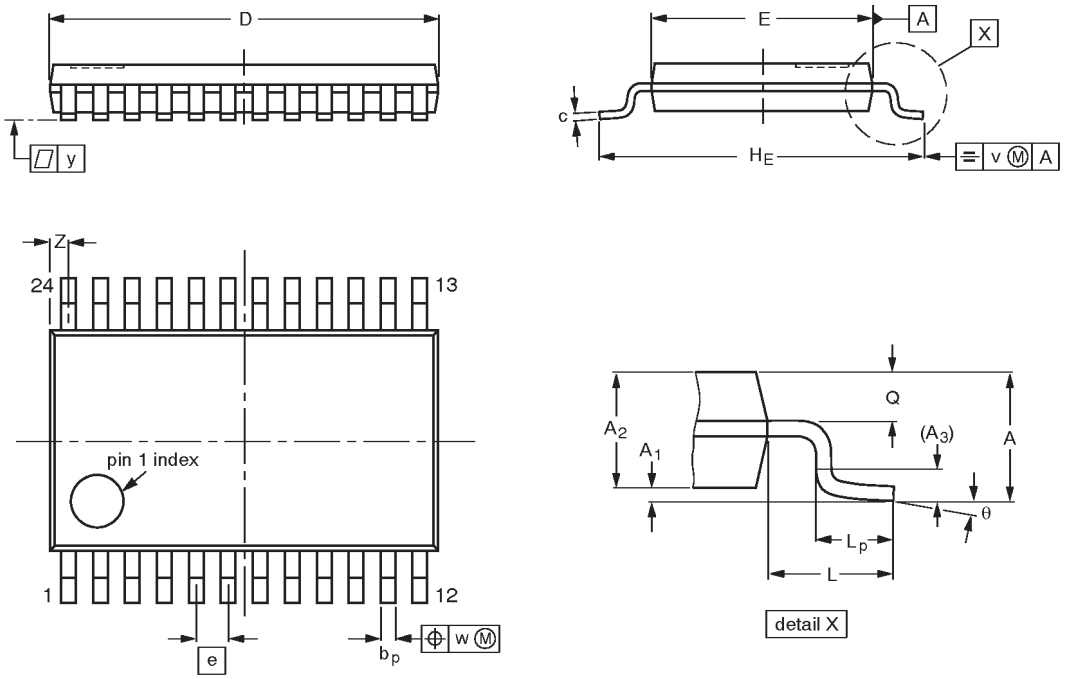
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

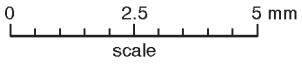
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm SOT355-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

print code Date of release: 05-96

Document order number: 9397-750-03537

Let's make things better.

Philips Semiconductors

PHILIPS